



## TITLE OF THE INVENTION

## DIELECTRIC DEVICE

## BACKGROUND OF THE INVENTION

## 5 Field of the Invention

The present invention relates to a dielectric device having a dielectric film.

## Description of the Background Art

10 A memory having a capacitor composed of a ferroelectric film (generally referred to as a dielectric capacitor) provided in a gate portion in a field effect transistor (FET) has been known as a nondestructive readable nonvolatile memory. As the structure of such a ferroelectric memory, an  
15 MFS (metal-ferroelectrics- semiconductor) structure, an MFIS (metal-ferroelectrics-insulator-semiconductor) structure, an MFMIS (metal-ferroelectrics-metal-insulator-semiconductor) structure, and so forth have been proposed.

Fig. 12 is a schematic cross-sectional view showing an  
20 example of the ferroelectric memory having the MFMIS structure. The ferroelectric memory shown in Fig. 12 is disclosed in JP-A-5-327062, for example.

In Fig. 12, a source region 34 composed of a  $p^+$  layer and a drain region 35 composed of a  $p^+$  layer are formed with  
25 predetermined spacing on the surface of an  $n^+$  silicon

substrate 31. A region of the silicon substrate 31 between the source region 34 and the drain region 35 is a channel region 36. A gate insulating film 32 is formed on the channel region 36, and a gate electrode 33 is formed on the gate  
5 insulating film 32.

An interlayer insulating film 37 is formed on the silicon substrate 31 and the gate electrode 33. A contact hole 39 is formed in the interlayer insulating film 37 on the gate electrode 33, and an interconnection layer 40 is formed  
10 in the contact hole 39.

A contact hole is provided in the interlayer insulating film 37 on each of the source region 34 and the drain region 35, and interconnection layers 45 and 46 are respectively formed in the contact holes. A lower electrode 42 is formed  
15 on the interconnection layer 40 connected to the gate electrode 33. A ferroelectric film 43 is formed on the lower layer 42, and an upper electrode 44 is formed on the ferroelectric film 43. Further, ohmic electrodes 47 and 48 are respectively formed on the interconnection layers 45 and  
20 46 connected to the source region 34 and the drain region 35.

In the ferroelectric memory, the lower electrode 42, the ferroelectric film 43, and the upper electrode 44 constitute a ferroelectric capacitor.

In the ferroelectric memory shown in Fig. 12, the lower  
25 electrode 42 and the upper electrode 44 are formed of a metal

which is low in reactivity, for example, Pt (platinum). Since the ferroelectric film 43 is thus formed on the lower electrode 42 composed of the metal which is low in reactivity, and the interlayer insulating film 37 is provided around the interconnection layer 40 between the gate electrode 33 and the lower electrode 42, constituent atoms are sufficiently prevented from reacting with each other and mutually diffusing between the ferroelectric film 43 and the silicon substrate 31.

10 In the structure of the above-mentioned conventional ferroelectric memory, when heat treatment is performed in a step subsequent to the formation of the ferroelectric capacitor, however, grain boundaries of columnar crystals are formed in Pt which is the material for the lower electrode 15 42 and the upper electrode 44, so that oxygen in the ferroelectric film 43 is easily diffused in Pt. Consequently, an oxidized layer is formed in the vicinity of a surface, in contact with the lower electrode 42, of the interconnection layer 40, so that the resistance of the 20 interconnection layer 40 is increased.

When the dielectric capacitor is placed in an atmosphere including hydrogen at the time of forming an insulating film in the subsequent step, the desorption of oxygen from the ferroelectric film 43 is speeded up by the catalytic action 25 of Pt. Consequently, a degraded layer is formed in the

vicinity of a surface, in contact with the upper electrode 44, of the ferroelectric film 43. From the foregoing results, the polarization characteristics of the ferroelectric film 43 are degraded.

5       Pt which is the material for the lower electrode 42 and the upper electrode 44 is low in reactivity, and has difficult etching characteristics, so that the ferroelectric memory takes long to process, and is low in productivity. Further, Pt is expensive, so that the material cost and the fabrication  
10 cost of the ferroelectric memory are increased.

An object of the present invention is to provide a dielectric device which has good polarization characteristics and can be improved in productivity and lowered in cost.

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#### SUMMARY OF THE INVENTION

A dielectric device according to the present invention comprises first and second impurity regions formed with predetermined spacing on a semiconductor,  
20 a gate insulating film formed on a region between the first and second impurity regions, a gate electrode formed on the gate insulating film, an interlayer insulating film formed on the semiconductor so as to cover the gate electrode and the gate insulating film and having a contact hole, a lower  
25 electrode layer formed in the contact hole of the interlayer

insulating film and electrically connected to the gate electrode, a dielectric film formed on the interlayer insulating film so as to be brought into contact with the upper surface of the lower electrode layer, and an upper  
5 electrode layer formed on the dielectric film, the lower electrode layer and the upper electrode layer being composed of a conductive oxide having a perovskite structure, the dielectric film being composed of dielectrics having a perovskite structure.

10 In the dielectric device, the lower electrode layer, the upper electrode layer and the dielectric film respectively have perovskite structures, and are similar in crystalline structure. Consequently, lattice matching between the lower electrode layer and the dielectric film and lattice matching  
15 between the dielectric film and the upper electrode layer are improved, so that the crystallizability of the dielectric film formed on the lower electrode layer is improved, and interface stability between the lower electrode layer and the dielectric film and interface stability between the  
20 dielectric film and the upper electrode layer are improved. There occurs no desorption of elements constituting the dielectric film (for example, oxygen) by the catalytic action of the lower electrode layer and the upper electrode layer. Consequently, good polarization characteristics are  
25 obtained in the dielectric film.

The conductive oxide having a perovskite structure is easy to process, and can be also formed in continuous processes in a fabricating apparatus which is also used for fabricating the dielectric film having a perovskite  
5 structure. Further, the conductive oxide having a perovskite structure can be formed at lower cost, as compared with a platinum Group metal.

Particularly, the lower electrode layer which is brought into contact with the lower surface of the dielectric  
10 film is provided in the contact hole of the interlayer insulating film. In patterning the upper electrode layer and the dielectric film, therefore, a material for the lower electrode layer does not adhere or deposit on sidewalls of the dielectric film. Even when a material for the upper  
15 electrode layer adheres or deposits on the sidewalls of the dielectric film, the lower electrode layer is provided in the contact hole of the interlayer insulating film, so that no current leaks between the upper electrode layer and the lower electrode layer. Consequently, the reliability and the yield  
20 of the dielectric device are prevented from being decreased by the adhesion or the deposition of the conductive material on the sidewalls of the dielectric film.

Consequently, a dielectric memory which has good device characteristics and can be improved in productivity and  
25 lowered in cost is obtained.

The dielectric device may further comprise a connecting layer formed under the lower electrode layer in the contact hole for electrically connecting the lower electrode layer to the gate electrode.

5        In this case, the connecting layer and the lower electrode layer are provided in the contact hole of the interlayer insulating film, so that the lower electrode layer in the contact hole is electrically connected to the gate electrode by the connecting layer.

10       The upper electrode layer and the lower electrode layer may be composed of a layered structure conductive oxide, and the dielectric film may be composed of layered structure dielectrics.

      In this case, the upper electrode layer, the lower  
15 electrode layer and the dielectric film respectively have layered structures, so that lattice matching between the lower electrode layer and the dielectric film and lattice matching between the dielectric film and the upper electrode layer are further improved. Accordingly, the  
20 crystallizability of the dielectric film formed on the lower electrode layer is further improved, and interface stability between the lower electrode layer and the dielectric film and interface stability between the dielectric film and the upper electrode layer are further improved. Therefore, better  
25 polarization characteristics are obtained in the dielectric

film.

The upper electrode layer and the lower electrode layer may be composed of a bismuth based system layered structure conductive oxide, and the dielectric film may be composed of  
5 layered structure dielectrics containing bismuth.

In this case, the upper electrode layer, the lower electrode layer and the dielectric film respectively have layered structures and contain bismuth, so that the upper electrode layer, the lower electrode layer and the dielectric  
10 film are similar in crystalline structure and are similar in constituent elements. Consequently, lattice matching between the lower electrode layer and the dielectric film and lattice matching between the dielectric film and the upper electrode layer are further improved, and a degraded layer  
15 is prevented from being formed by mutual diffusion of the constituent elements between the lower electrode layer and the dielectric film and between the dielectric film and the upper electrode layer. Accordingly, the crystallizability of the dielectric film formed on the lower electrode layer  
20 is further improved, and interface stability between the lower electrode layer and the dielectric film and interface stability between the dielectric film and the upper electrode layer are further improved. Consequently, better polarization characteristics are further obtained in the  
25 dielectric film.

The dielectric film may be composed of ferroelectrics. In this case, a ferroelectric device which has good device characteristics and can be improved in productivity and lowered in cost is realized.

5       The upper electrode layer and the lower electrode layer may be composed of a layered structure conductive oxide containing bismuth, strontium, copper and oxygen, and the dielectric film may be composed of layered structure ferroelectrics containing strontium, bismuth, tantalum and  
10 oxygen.

In this case, the upper electrode layer, the lower electrode layer and the dielectric film respectively have layered structures and contain bismuth, strontium and oxygen, so that the upper electrode layer, the lower  
15 electrode layer and the dielectric film are similar in crystalline structure and are similar in constituent elements. Consequently, lattice matching between the lower electrode layer and the dielectric film and lattice matching between the dielectric film and the upper electrode layer are  
20 further improved, and a degraded layer is prevented from being formed by mutual diffusion of the constituent elements between the lower electrode layer and the dielectric film and between the dielectric film and the upper electrode layer. Accordingly, the crystallizability of the dielectric film  
25 formed on the lower electrode layer is further improved, and

interface stability between the lower electrode layer and the dielectric film and interface stability between the dielectric film and the upper electrode layer are further improved. Therefore, a ferroelectric device which has better  
5 device characteristics and can be improved in productivity and lowered in cost is realized.

The dielectric device may further comprise a diffusion barrier layer provided between the connecting layer and the lower electrode layer. The dielectric device may further  
10 comprise a platinum layer provided between the diffusion barrier layer and the lower electrode layer.

A dielectric device according to another aspect of the present invention comprises a dielectric film composed of layered structure dielectrics containing bismuth, and a  
15 first electrode layer laminated on one surface of the dielectric film and composed of a bismuth based system layered structure conductive oxide.

In this case, both the dielectric film and the first electrode layer respectively have layered structures and  
20 contain bismuth, so that the dielectric film and the first electrode layer are similar in crystalline structure and are similar in constituent elements. Consequently, lattice matching between the dielectric film and the first electrode layer is further improved, and a degraded layer is prevented  
25 from being formed by mutual diffusion of the constituent

elements between the dielectric film and the first electrode layer. Accordingly, the crystallizability of the dielectric film in contact with the first electrode layer is further improved, and interface stability between the dielectric  
5 film and the first electrode layer is further improved. Therefore, better polarization characteristics are obtained in the dielectric film.

The dielectric film may be composed of ferroelectrics. In this case, a ferroelectric device which has good device  
10 characteristics and can be improved in productivity and lowered in cost is realized.

The dielectric film may be composed of layered structure ferroelectrics containing strontium, bismuth, tantalum and oxygen, and the first electrode layer may be composed of a  
15 layered structure conductive oxide containing bismuth, strontium, copper and oxygen.

In this case, both the dielectric film and the first electrode layer respectively have layered structures and contain bismuth, strontium and oxygen, so that the dielectric  
20 film and the first electrode layer are similar in crystalline structure and are similar in constituent elements. Consequently, lattice matching between the dielectric film and the first electrode layer is further improved, and a degraded layer is prevented from being formed by mutual  
25 diffusion of the constituent elements between the dielectric

film and the first electrode layer. Accordingly, the crystallizability of the dielectric film in contact with the first electrode layer is further improved, and interface stability between the dielectric film and the first electrode  
 5 layer is further improved. Therefore, a ferroelectric device which has better device characteristics and can be improved in productivity and lowered in cost is realized.

A dielectric device according to further aspect of the present invention comprises a dielectric film and a first  
 10 electrode layer laminated on one surface of the dielectric film, the dielectric film being composed of  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ ,  $(\text{Bi}_2\text{O}_2)^{2+}(\text{A}_{n-1}\text{B}_n\text{O}_{3n+1})^{2-}$ , where A is Sr, Ca, Ba, Pb, Bi, K or Na, and B is Ti, Ta, Nb, W or V,  $\text{Pb}(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$  ( $0 \leq x \leq 1$ ),  $(\text{Pb}_{1-x}\text{La}_x)(\text{Zr}_x\text{Ti}_{1-x})\text{O}_3$  ( $0 \leq x \leq 1$ ,  $0 \leq y \leq 1$ ),  $(\text{Sr}_{1-x}\text{Ca}_x)\text{TiO}_3$  ( $0 \leq x \leq 1$ ),  $(\text{Sr}_{1-x}\text{Ba}_x)\text{TiO}_3$  ( $0 \leq x \leq 1$ ),  $(\text{Sr}_{1-x-y}\text{Ba}_x\text{M}_y)\text{Ti}_{1-z}\text{N}_z\text{O}_3$ , where M is La, Bi, Sb or Y, and N is Nb, V, Ta, Mo or W,  $0 \leq x \leq 1$ ,  $y = 1 - x$ ,  $0 \leq z \leq 1$ ,  $\text{Sr}_2\text{Nb}_2\text{O}_7$ ,  $\text{Sr}_2\text{Ta}_2\text{O}_7$ ,  $\text{Pb}_5\text{Ge}_3\text{O}_{11}$ , or  $(\text{Pb}, \text{Ca})\text{TiO}_3$ , the first  
 15 electrode layer being composed of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ ,  $\text{A}_2\text{B}_2\text{C}_n\text{M}_{n+1}\text{O}_{2n+6}$ , where  $n = 0, 1, 2, 3, 4, 5$ , A is Tl, Bi, Mg or Cu, B is Ba, C is Ca, and M is Cu,  $(\text{Sr}, \text{La})\text{MO}_3$ , where M is Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ru or Ir,  $(\text{Sr}, \text{La})_2\text{MO}_4$ , where M is Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ru or Ir,  $\text{CaMO}_3$ , where M is V, Cr, Fe or Ru,  $\text{LuNiO}_3$ ,  $\text{Ba}(\text{Pb}, \text{Bi})\text{O}_3$ ,  $\text{LnBa}_2\text{Cu}_n\text{O}_{n+4-a}$ , where  $n = 3, 4$ , Ln is Y, La, Pr, Nd, Sm, Eu, Gd, Td, Dy, Ho, Er, Tm, Yb or Lu,  $(\text{Ba}, \text{A})\text{BiO}_3$ , where A is K or Rb,  $\text{Sr}_{1+n}\text{Cu}_n\text{O}_{2n+1}$ , where  
 20

$n = 1, 2, 3, \infty$ ,  $\text{ReO}_3$ , or  $\text{M}_x\text{WO}_3$ , where M is H, an alkali metal, an alkaline earth metal, Cu, Ag, In, Tl, Sn or Pb.

The dielectric device may further comprise first and second impurity regions formed with predetermined spacing on a semiconductor, and the dielectric film may be formed on a region between the first and second impurity regions.

In this case, a dielectric memory which has good device characteristics and can be improved in productivity and lowered in cost is realized.

The dielectric device may further comprise first and second impurity regions formed with predetermined spacing on a semiconductor, and a gate insulating film formed on a region between the first and second impurity regions, and the dielectric film may be formed on the gate insulating film.

In this case, a dielectric memory which has good device characteristics and can be improved in productivity and lowered in cost is realized.

The dielectric device may further comprise a second electrode layer laminated on the other surface of the dielectric film, and the second electrode layer may have a crystalline structure similar to that of the dielectric film.

In this case, the dielectric film and the first and second electrode layers are similar in crystalline structure. Consequently, lattice matching between the first electrode layer and the dielectric film and lattice matching

between the dielectric film and the second electrode layer are improved, so that the crystallizability of the dielectric film formed between the first electrode layer and the second electrode layer is improved, and interface stability between  
5 the first electrode layer and the dielectric film and interface stability between the dielectric film and the second electrode layer are improved. Therefore, a dielectric device having good device characteristics is realized.

The second electrode layers may be composed of a bismuth  
10 based system layered structure conductive oxide.

In this case, the dielectric film and the first and second electrode layers respectively have layered structures and contain bismuth, so that the dielectric film and the first and second electrode layers are similar in crystalline  
15 structure and are similar in constituent elements.

Consequently, lattice matching between the first electrode layer and the dielectric film and lattice matching between the dielectric film and the second electrode layer are further improved, and a degraded layer is prevented from  
20 being formed by mutual diffusion of the constituent elements between the first electrode layer and the dielectric film and between the dielectric film and the second electrode layer. Accordingly, the crystallizability of the dielectric film formed between the first electrode layer and the second  
25 electrode layer is further improved, and interface stability

between the first electrode layer and the dielectric film and interface stability between the dielectric film and the second electrode layer are further improved. Therefore, better polarization characteristics are obtained in the dielectric film.

The dielectric film may be composed of ferroelectrics. In this case, a ferroelectric device which has good device characteristics and can be improved in productivity and lowered in cost is realized.

The dielectric film may be composed of layered structure ferroelectrics containing strontium, bismuth, tantalum and oxygen, and the first and second electrode layers may be composed of a layered structure conductive oxide containing bismuth, strontium, copper and oxygen.

In this case, the dielectric film and the first and second electrode layers respectively have layered structures and contain bismuth, strontium and oxygen, so that the dielectric film and the first and second electrode layers are similar in crystalline structure and are similar in constituent elements. Consequently, lattice matching between the first electrode layer and the dielectric film and lattice matching between the dielectric film and the second electrode layer are further improved, and a degraded layer is prevented from being formed by mutual diffusion of the constituent elements between the first electrode layer and

the dielectric film and between the dielectric film and the second electrode layer. Accordingly, the crystallizability of the dielectric film formed between the first electrode layer and the second electrode layer is further improved, and interface stability between the first electrode layer and the dielectric film and interface stability between the dielectric film and the second electrode layer are further improved. Therefore, a ferroelectric device which has better device characteristics and can be improved in productivity and lowered in cost is realized.

The second electrode layer is composed of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ ,  $\text{A}_2\text{B}_2\text{C}_n\text{M}_{n+1}\text{O}_{2n+6}$ , where  $n = 0, 1, 2, 3, 4, 5$ , A is Tl, Bi, Mg or Cu, B is Ba, C is Ca, and M is Cu,  $(\text{Sr}, \text{La})\text{MO}_3$ , where M is Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ru or Ir,  $(\text{Sr}, \text{La})_2\text{MO}_4$ , where M is Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ru or Ir,  $\text{CaMO}_3$ , where M is V, Cr, Fe or Ru,  $\text{LuNiO}_3$ ,  $\text{Ba}(\text{Pb}, \text{Bi})\text{O}_3$ ,  $\text{LnBa}_2\text{Cu}_n\text{O}_{n+4-a}$ , where  $n = 3, 4$ , Ln is Y, La, Pr, Nd, Sm, Eu, Gd, Td, Dy, Ho, Er, Tm, Yb or Lu,  $(\text{Ba}, \text{A})\text{BiO}_3$ , where A is K or Rb,  $\text{Sr}_{1+n}\text{Cu}_n\text{O}_{2n+1}$ , where  $n = 1, 2, 3, \infty$ ,  $\text{ReO}_3$ , or  $\text{M}_x\text{WO}_3$ , where M is H, an alkali metal, an alkaline earth metal, Cu, Ag, In, Tl, Sn or Pb.

The dielectric film may further comprise first and second impurity regions formed with predetermined spacing on a semiconductor, and a gate insulating film formed on a region between the first and second impurity regions, and the second electrode layer may be formed on the gate insulating film.

In this case, a dielectric memory which has good device characteristics and can be improved in productivity and lowered in cost is realized.

The foregoing and other objects, features, aspects and  
5 advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

#### 10 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross-sectional view showing the structure of a ferroelectric memory in the first embodiment of the present invention;

Fig. 2 is a schematic view showing a crystalline  
15 structure of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ , which is a material for a lower electrode and an upper electrode in the ferroelectric memory shown in Fig. 1;

Fig. 3 is a schematic view showing a crystalline structure of  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ , which is a material for a  
20 ferroelectric film in the ferroelectric memory shown in Fig. 1;

Fig. 4 is a cross-sectional view showing the steps of a method of fabricating the ferroelectric memory shown in Fig. 1;

25 Fig. 5 is a cross-sectional view showing the steps of

the method of fabricating the ferroelectric memory shown in Fig. 1;

Fig. 6 is a cross-sectional view showing the steps of the method of fabricating the ferroelectric memory shown in  
5 Fig. 1;

Fig. 7 is a cross-sectional view showing the steps of the method of fabricating the ferroelectric memory shown in Fig. 1;

Fig. 8 is a cross-sectional view showing the steps of  
10 the method of fabricating the ferroelectric memory shown in Fig. 1;

Fig. 9 is schematic cross-sectional view showing the structure of a ferroelectric memory in the second embodiment of the present invention;

15 Fig. 10 is a schematic cross-sectional view showing the structure of a ferroelectric memory in the third embodiment of the present invention;

Fig. 11 is a schematic cross-sectional view showing the structure of a ferroelectric memory in the fourth embodiment  
20 of the present invention; and

Fig. 12 is a schematic cross-sectional view showing an example of a conventional ferroelectric memory.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

25 (1) First Embodiment

Fig. 1 is a schematic cross-sectional view showing the structure of a ferroelectric memory in the first embodiment of the present invention.

In Fig. 1, a source region 4 composed of an  $n^+$  layer and  
5 a drain region 5 composed of an  $n^+$  layer are formed with predetermined spacing on the surface of a p-type single crystalline silicon substrate 1. A region of the silicon substrate 1 between the source region 4 and the drain region 5 is a channel region 6.

10 A gate insulating film 2 composed of  $\text{SiO}_2$  is formed on the channel region 6. A gate electrode 3 composed of polysilicon is formed on the gate insulating film 2. An interlayer insulating film 7 is formed on the silicon substrate 1 so as to cover the gate electrode 3 and the gate  
15 insulating film 2. A buffer layer 8 composed of  $\text{TiO}_2$  (titanium oxide),  $\text{CeO}_2$  (cerium oxide), etc. is formed on the interlayer insulating film 7.

A contact hole 9 is formed in the interlayer insulating film 7 on the gate electrode 3 and the buffer layer 8. A  
20 connecting layer (a plug) 10 composed of a conductive material such as polysilicon or W (tungsten) is formed up to a predetermined depth in the contact hole 9.

A diffusion barrier layer 11 composed of a conductive material such as TiN or TaSiN is formed on the connecting  
25 layer 10 in the contact hole 9, and a Pt layer 12a is formed

on the diffusion barrier layer 11.

A lower electrode 12 composed of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  (BSCO) which is a Bi (bismuth) based system conductive oxide is formed on the Pt layer 12a in the contact hole 9. A ferroelectric film 5 13 composed of  $\text{SrBi}_2\text{Ta}_2\text{O}_9$  (SBT) which is layered structure ferroelectrics having a perovskite crystalline structure is formed on the buffer layer 8 so as to be brought into contact with the upper surface of the lower electrode 12. An upper electrode 14 composed of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  which is a Bi based system 10 conductive oxide is formed on the ferroelectric film 13.

A contact hole is formed in the buffer layer 8 and the interlayer insulating film 7 on each of the source region 4 and the drain region 5, and a source electrode 15 and a drain electrode 16 which are composed of a conductive material such 15 as polysilicon are respectively formed in the contact holes. Interconnection layers 17 and 18 are respectively formed on the source electrode 15 and the drain electrode 16.

In the ferroelectric memory shown in Fig. 1, the lower electrode 12, the ferroelectric film 13, and the upper 20 electrode 14 constitute a ferroelectric capacitor.

In the present embodiment, the lower electrode 12 corresponds to a lower electrode layer or a first conductive layer, and the upper electrode 14 corresponds to an upper electrode layer or a second conductive layer.

25 Fig. 2 is a schematic view showing a crystalline

structure of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  which is the material for the lower electrode 12 and the upper electrode 14 in the ferroelectric memory shown in Fig. 1. Fig. 3 is a schematic view showing a crystalline structure of  $\text{SrBi}_2\text{Ta}_2\text{O}_6$ , which is the material for the ferroelectric film 13 in the ferroelectric memory shown in Fig. 1.

As shown in Fig. 2,  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  is a layered structure conductive oxide having a perovskite crystalline structure.  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  can be formed at a temperature of approximately  $600^\circ\text{C}$ , exhibits superconductivity at low temperature, and has a specific resistance at room temperature of approximately  $10^{-4} \Omega\text{cm}$ . On the other hand, as shown in Fig. 3,  $\text{SrBi}_2\text{Ta}_2\text{O}_6$  is layered structure ferroelectrics having a perovskite crystalline structure. Both the in-plane lattice constants of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  and  $\text{SrBi}_2\text{Ta}_2\text{O}_6$ , are 0.39 nm.  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  shown in Fig. 2 and  $\text{SrBi}_2\text{Ta}_2\text{O}_6$ , shown in Fig. 3 are similar in crystalline structure.

Consequently, lattice matching between the lower electrode 12 and the ferroelectric film 13 and lattice matching between the ferroelectric film 13 and the upper electrode 14 are improved. Further, the crystallizability of the ferroelectric film 13 formed on the lower electrode 12 is improved.

Elements constituting  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  are Sr, Bi, Cu and O, as shown in Fig. 2. On the other hand, elements constituting

$\text{SrBi}_2\text{Ta}_2\text{O}_6$ , are Sr, Bi, Ta and O, as shown in Fig. 3.  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ , shown in Fig. 2 and  $\text{SrBi}_2\text{Ta}_2\text{O}_6$ , shown in Fig. 3 are similar in constituent elements.

Consequently, the vicinity of the surface of the lower  
5 electrode 12 with the ferroelectric film 13 and the vicinity  
of the surface of the ferroelectric film 13 with the upper  
electrode 14 are hardly affected by mutual diffusion of the  
constituent elements. That is, when Cu in the lower electrode  
12 and the upper electrode 14 and Ta in the ferroelectric film  
10 13 mutually diffuse,  $\text{SrBi}_2\text{Ta}_2\text{O}_6$ , which is the material for the  
ferroelectric film 13 is partially formed in the vicinity of  
the surface of and on the inside of the lower electrode 12  
and the vicinity of the surface of and on the inside of the  
upper electrode 14, and  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ , which is the material for  
15 the lower electrode 12 and the upper electrode 14 is partially  
formed in the vicinity of the surface of and on the inside  
of the ferroelectric film 13. In this case, the surface of  
the lower electrode 12 with the ferroelectric film 13 and the  
surface of the ferroelectric film 13 with the upper electrode  
20 14 are slightly disturbed, so that no degraded layer is formed  
on the surfaces.

The ferroelectric capacitor which is constituted by the  
lower electrode 12, the ferroelectric film 13 and the upper  
electrode 14 has a whole oxide type laminated structure, so  
25 that interface stability is improved, and oxygen is

prevented from being desorbed by the catalytic action of Pt. Even if degradation such as oxygen deficiency occurs in the ferroelectric film 13, the characteristics of the lower electrode 12, the ferroelectric film 13 and the upper electrode 14 can be recovered by performing heat treatment for supplying oxygen. From the foregoing results, a ferroelectric capacitor having superior polarization fatigue characteristics is formed.

The lower electrode 12, the ferroelectric film 13 and the upper electrode 14 can be formed by continuous processes in a common fabricating apparatus, so that the productivity of the ferroelectric memory is improved. For example, when the lower electrode 12 and the upper electrode 14 are formed using a sputter target having a diameter of 6 inches which is composed of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ , the material cost is one-tenth that in a case where they are formed using a sputter target having a diameter of 6 inches which is composed of Pt. As a result, the cost of the ferroelectric memory is lowered.

Furthermore,  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  which is the material for the lower electrode 12 and the upper electrode 14 is high in reactivity, so that it is superior in processibility and can be also easily etched by chemical etching. Etching to which reactivity is applied is also possible by introducing  $\text{Cl}_2$  or  $\text{HBr}$  into an etching reaction system. As a result, the etching speed can be increased. Further, the lower electrode 12, the

ferroelectric film 13 and the upper electrode 14 can be also simultaneously etched. From the foregoing results, the productivity of the ferroelectric memory is improved.

Figs. 4 to 8 are cross-sectional views showing the steps of a method of fabricating the ferroelectric memory shown in Fig. 1.

First, as shown in Fig. 4 (a), a gate insulating film 2 composed of  $\text{SiO}_2$  having a thickness of 100 Å is formed on a p-type silicon substrate 1 by a thermal oxidation method, and a gate electrode 3 composed of polysilicon having a thickness of 2000 Å is formed on the gate insulating film 2 by a CVD (Chemical Vapor Deposition) method.

As shown in Fig. 4 (b), the gate electrode 3 and the gate insulating film 2 in a portion excluding a gate forming region on the silicon substrate 1 are then removed using a dry process such as reactive ion etching (RIE) or ion milling, to form a gate portion. N-type impurities (an n-type dopant) are ion-implanted into the surface of the silicon substrate 1 using the gate electrode 3 as a mask for ion implantation, to perform heat treatment. Consequently, a source region 4 and a drain region 5 which are composed of an n-type impurity layer (an  $n^+$  layer) are respectively formed in self-alignment with the gate insulating film 2 and the gate electrode 3 on the silicon substrate 1. A region of the silicon substrate 1 between the source region 4 and the drain region 5 is a

channel region 6.

Thereafter, an interlayer insulating film 7 composed of  $\text{SiO}_2$ , etc. having a thickness of approximately 6000 Å is formed by a CVD method or the like on the silicon substrate 1 so as to cover the gate electrode 3 and the gate insulating film 2, as shown in Fig. 4 (c).

As shown in Fig. 5 (d), a buffer layer 8 composed of  $\text{TiO}_2$ ,  $\text{CeO}_2$ , etc. having a thickness of 500 Å is formed on the interlayer insulating film 7. Thereafter, a contact hole 9 is provided in the buffer layer 8 and the interlayer insulating film 7 on the gate electrode 3 by a lithographic technique, as shown in Fig. 5 (e).

As shown in Fig. 5 (f), a connecting layer 10 composed of a conductive material such as polysilicon or W is formed in the contact hole 9. In this case, the thickness of the connecting layer 10 is set such that the distance from an upper end of the contact hole 9 to the upper surface of the connecting layer 10 is 1500 Å. As a method of forming the connecting layer 10, a conductive layer is formed on the inside of the contact hole 9 and the whole surface of the buffer layer 8, after which the whole surface is etched, to remove the conductive layer on the buffer layer 8.

As shown in Fig. 6 (g), a diffusion barrier layer 11 composed of a conductive material such as TiN or TaSiN is then formed on the inside of the contact hole 9 and the whole

surface of the buffer layer 8 by a sputtering method or the like in order to prevent the connecting layer 10 from being oxidized and prevent impurities from being diffused into a gate portion.

5       As shown in Fig. 6 (h), the whole surface of the diffusion barrier layer 11 is etched, to remove the diffusion barrier layer 11 on the buffer layer 8 as well as to etch the buffer layer 11 back until the upper surface of the diffusion barrier layer 11 in the contact hole 9 is lower than the upper  
10 surface of the buffer layer 8. In this case, mixed gas of  $\text{BCl}_3$  and  $\text{Cl}_2$  is used as etching gas, and the etching conditions are an RF power of 250 W and a pressure of  $2 \times 10^{-2}$  Torr. The other gas such as Ar or  $\text{N}_2$  may be mixed with the mixed gas. The diffusion barrier layer 11 having a thickness of 300 Å  
15 is thus formed on the connecting layer 10 in the contact hole 9.

As shown in Fig. 6 (i), a Pt film 12a is then formed on the buffer layer 8 and the diffusion barrier layer 11 in the contact hole 9 in order to improve the crystallizability of  
20  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  formed thereon.

Thereafter, as shown in Fig. 7 (j), the whole surface of the Pt layer 12a is etched, to remove the Pt layer 12a on the buffer layer 8, and the Pt layer 12 is etched back until the upper surface of the Pt layer 12a in the contact hole 9  
25 is lower than the upper surface of the buffer layer 8. In

this case, Ar is used as etching gas, and the etching conditions are an RF power of 300 W and a pressure of  $3 \times 10^{-3}$  Torr. The other gas such as  $\text{Cl}_2$ , HBr, or  $\text{BCl}_3$  may be used as etching gas, or their mixed gas may be used. The Pt layer 5 12a having a thickness of 200 Å is thus formed on the diffusion barrier layer 11 in the contact hole 9.

As shown in Fig. 7 (k), a lower electrode 12 composed of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$  is then formed by a sputtering method or the like on the buffer layer 8 and the Pt layer 12a in the contact hole 10 9.

Thereafter, the lower electrode 12 is flattened by etch-back, a CMP (Chemical Mechanical Polishing) method, or the like, leaving the lower electrode 12 only in the contact hole 9, to form the lower electrode 12 having a thickness of 15 1000 Å in the contact hole 9, as shown in Fig. 7 (l). In this case, Ar, Hbr, etc. is used as etching gas, and the etching conditions are an RF power of 200 to 400 W and a pressure of approximately  $1 \times 10^{-3}$  Torr.

In the steps shown in Figs. 6 (h) and 7 (j), the lower 20 electrode 12, the Pt layer 12a and the diffusion barrier layer 11 may be simultaneously flattened by etch-back or a CMP method after continuously forming the diffusion barrier layer 11, the Pt layer 12a and the lower electrode 12 instead of etching the diffusion barrier layer 11 and the Pt layer 25 12a back.

As shown in Fig. 8 (m), a ferroelectric film 13 composed of  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ , having a thickness of 2000 Å is then formed on the lower electrode 12 and the buffer layer 8 by a sputtering method or the like. Further, as shown in Fig. 8 (n), an upper electrode 14 composed of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ , having a thickness of 1500 Å is formed on the ferroelectric film 13 by a sputtering method or the like.

Thereafter, the upper electrode 14 and the ferroelectric film 13 are patterned by etching, as shown in Fig. 8 (o). In this case, Ar, HBr, etc. is used as etching gas, and the etching conditions are an RF power of 200 to 400 W and a pressure of approximately  $1 \times 10^{-3}$  Torr.

At the time of etching, the whole of the buffer layer 8 may be etched. The ferroelectric film 13 need not necessarily extend over the buffer layer 8, provided that it is in contact with the upper surface of the lower electrode 12.

As shown in Fig. 1, the buffer layer 8 and the interlayer insulating film 7 on each of the source electrode 4 and the drain electrode 5 are then provided with a contact hole, and a source electrode 15 and a drain electrode 16 which are composed of a conductive material such as polysilicon are respectively formed in the contact holes. Finally, interconnection layers 17 and 18 which are composed of Al are respectively formed on the source electrode 15 and the drain

electrode 16. The ferroelectric memory shown in Fig. 1 is thus fabricated.

In the ferroelectric memory according to the present embodiment, the lower electrode 12 is provided in the contact  
5 hole 9 in the interlayer insulating film 7. In patterning the upper electrode 14 and the ferroelectric film 13 by etching, therefore, the conductive material composing the lower electrode 12 does not deposit on the sidewalls of the ferroelectric film 13. As a result, the reliability and the  
10 yield of the ferroelectric memory are sufficiently prevented from being decreased by the deposition of the conductive material on the sidewalls of the ferroelectric film 13.

In the step shown in Fig. 8 (m), the ferroelectric film 13 is formed on the interlayer insulating film 7 through the  
15 buffer layer 8, so that the stress applied to the ferroelectric film 13 is retrieved by the buffer layer 8, thereby preventing the ferroelectric film 13 from being cracked as well as preventing the constituent elements from reacting with each other and mutually diffusing between the  
20 ferroelectric film 13 and the interlayer insulating film 7. As a result, the reliability and the yield of the ferroelectric memory are further improved.

Furthermore, the interlayer insulating film 7 is provided around the conductive layer 10 between the  
25 ferroelectric film 13 and the silicon substrate 1, so that

the constituent elements are sufficiently prevented from reacting with each other and mutually diffusing between the ferroelectric film 13 and the silicon substrate 1.

Description of the principle of operations performed by  
5 the ferroelectric memory shown in Fig. 1. A sufficient positive voltage to inversely polarize the ferroelectric film 13 is applied to the upper electrode 14, to set the voltage of the upper electrode 14 to zero again. Consequently, the surface of the ferroelectric film 13 with  
10 the upper electrode 14 is negatively charged, and the surface thereof with the lower electrode is positively charged.

In this case, the surface of the lower electrode 12 with the ferroelectric film 13 is negatively charged, and the surface of the gate electrode 3 with the gate insulating film  
15 2 is positively charged. As a result, an inversion layer is formed in the channel region 6 between the source region 4 and the drain region 5, so that a FET is turned on, although the voltage of the upper electrode 14 is zero.

Contrary to this, a sufficient negative voltage to  
20 inversely polarize the ferroelectric film 13 is applied to the upper electrode 14, to set the voltage of the upper electrode 14 to zero again. Consequently, the surface of the ferroelectric film 13 with the upper electrode 14 is positively charged, and the surface thereof with the lower  
25 electrode 12 is negatively charged.

In this case, the surface of the lower electrode 12 with the ferroelectric film 13 is positively charged, and the surface of the gate electrode 13 with the gate insulating film 2 is negatively charged. As a result, no inversion layer is formed in the channel region 6 between the source region 4 and the drain region 5, so that the FET is turned off.

When the ferroelectric film 13 is sufficiently polarized inversely, the FET can be selectively turned on or off even after the voltage applied to the upper electrode 14 is set to zero. Therefore, it is possible to discriminate between data "1" and "0" which are stored in the ferroelectric memory by detecting a current between the source and the drain of the FET.

## (2) Second Embodiment

Fig. 9 is a schematic cross-sectional view showing the MFMIS structure of a ferroelectric memory in the second embodiment of the present invention.

In Fig. 9, a source region 22 composed of an  $n^+$  layer and a drain region 23 composed of an  $n^+$  layer are formed with predetermined spacing on the surface of a p-type silicon substrate 21. A region of the silicon substrate 21 between the source region 22 and the drain region 23 is a channel region 24. A gate insulating film 25, a lower electrode 26, a ferroelectric film 27 and an upper electrode 28 are successively formed on the channel region 24.

In the ferroelectric memory shown in Fig. 9, the lower electrode 26, the ferroelectric film 27 and the upper electrode 28 constitute a ferroelectric capacitor. The lower electrode 26 and the upper electrode 28 are composed of  
5  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ , and the ferroelectric film 27 is composed of  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ .

The ferroelectric memory according to the present embodiment also has superior resistance to polarization degradation, and can be improved in productivity and lowered  
10 in cost, similarly to the ferroelectric memory according to the first embodiment.

### (3) Third Embodiment

Fig. 10 is a schematic cross-sectional view showing the MFIS structure of a ferroelectric memory in the third  
15 embodiment of the present invention.

In Fig. 10, a source region 22 composed of an  $n^+$  layer and a drain region 23 composed of an  $n^+$  layer are formed with predetermined spacing on the surface of a p-type silicon substrate 21. A region of the silicon substrate 21 between  
20 the source region 22 and the drain region 23 is a channel region 24. A gate insulating film 25, a ferroelectric film 27, and a gate electrode 28a are formed in this order on the channel region 24.

In the ferroelectric memory shown in Fig. 10, the  
25 channel region 24 in the p-type silicon substrate 21, the gate

insulating film 25, the ferroelectric film 27, and the gate electrode 28a constitute a ferroelectric capacitor. The ferroelectric film 27 is composed of  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ , and the gate electrode 28a is composed of

5  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ .

The ferroelectric memory according to the present embodiment also has superior resistance to polarization degradation, and can be improved in productivity and lowered in cost, similarly to the ferroelectric memory according to  
10 the first embodiment.

#### (4) Fourth Embodiment

Fig. 11 is a schematic cross-sectional view showing the MFS structure of a ferroelectric memory in the fourth embodiment of the present invention.

15 In Fig. 11, a source region 22 composed of an  $n^+$  layer and a drain region 23 composed of an  $n^+$  layer are formed with predetermined spacing on the surface of a p-type silicon substrate 21. A region of the silicon substrate 21 between the source region 22 and the drain region 23 is a channel  
20 region 24. A ferroelectric film 27 and a gate electrode 28a are formed in this order on the channel region 24.

In the ferroelectric memory shown in Fig. 11, the channel region 24 in the p-type silicon substrate 21, the ferroelectric film 27 and the gate electrode 28a constitute  
25 a ferroelectric capacitor. The ferroelectric film 27 is

composed of  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ , and the gate electrode 28a is composed of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ .

The ferroelectric memory according to the present embodiment also has superior resistance to polarization degradation, and can be improved in productivity and lowered in cost, similarly to the ferroelectric memory according to the first embodiment.

#### (5) Another Application

The present invention is also applicable to a ferroelectric memory having a structure shown in Fig. 12. In this case, a lower electrode 42 and an upper electrode 44 are composed of  $\text{Bi}_2\text{Sr}_2\text{CuO}_6$ , and a ferroelectric film 43 is composed of  $\text{SrBi}_2\text{Ta}_2\text{O}_9$ .

#### (6) Another Electrode Material

As a material for the lower electrodes 12, 26 and 42, the upper electrodes 14, 28 and 44, and the gate electrode 28a, a conductive oxide composed of each of the following materials can be used.

##### ① Perovskite material

•  $\text{A}_2\text{B}_2\text{C}_n\text{M}_{n+1}\text{O}_{2n+6}$

$n = 0, 1, 2, 3, 4, 5$ . A is Tl (thallium), Bi, Mg or Cu.

B is Ba, C is Ca, and M is Cu.

•  $(\text{Sr}, \text{La})\text{MO}_3$

•  $(\text{Sr}, \text{La})_2\text{MO}_4$

M is Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ru or Ir.

- $\text{CaMO}_3$

M is V, Cr, Fe or Ru.

- $\text{LuNiO}_3$

- $\text{Ba(Pb, Bi)O}_3$

- 5 •  $\text{LnBa}_2\text{Cu}_n\text{O}_{n+4-a}$

$n = 3, 4$ . Ln is Y, La, Pr, Nd, Sm, Eu, Gd, Td, Dy, Ho, Er, Tm, Yb or Lu.

- $(\text{Ba, A})\text{BiO}_3$

A is K or Rb.

- 10 •  $\text{Sr}_{1+n}\text{Cu}_n\text{O}_{2n+1}$

$n = 1, 2, 3, \infty$ .

It is preferable to use the perovskite material in the above-mentioned item ①, and more preferable to use the perovskite material indicated by  $\text{A}_2\text{B}_2\text{C}_n\text{M}_{n+1}\text{O}_{2n+6}$ .

- 15 As the material for the lower electrodes 12, 26 and 42, the upper electrodes 14, 28 and 44, and the gate electrode 28a, a conductive oxide composed of each of the following materials can be also used.

- ②  $\text{ReO}_3$  material

- 20 •  $\text{ReO}_3$

- ③  $\text{M}_x\text{WO}_3$  material

M is H, an alkali metal, an alkaline earth metal, Cu, Ag, In, Tl, Sn or Pb.

- The lower electrodes 12, 26 and 42, the upper electrodes 14, 28 and 44, and the gate electrode 28a may have a

multilayered structure of the above-mentioned materials.

(7) Another ferroelectric material

Ferroelectrics composed of each of the following materials may be used as the ferroelectric films 13, 27 and 5 43.

① Bismuth based system layered structure

ferroelectrics expressed by the following general formula:



A is Sr, Ca, Ba, Pb, Bi, K or Na, and B is Ti, Ta, Nb, 10 W or V.

In the case of  $n = 1$  :

- $\text{Bi}_2\text{WO}_6$
- $\text{Bi}_2\text{VO}_{5.5}$

In the case of  $n = 2$  :

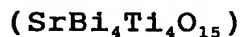
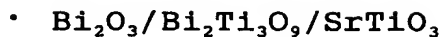
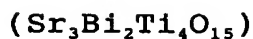
- 15
- $\text{Bi}_2\text{O}_3/\text{SrTa}_2\text{O}_6$
  - $(\text{SrBi}_2\text{Ta}_2\text{O}_9)$  : SBT
  - $\text{Bi}_2\text{O}_3/\text{SrNb}_2\text{O}_6$
  - $(\text{SrBi}_2\text{Nb}_2\text{O}_9)$

In the case of  $n = 3$  :

- 20
- $\text{Bi}_2\text{O}_3/\text{SrTa}_2\text{O}_6/\text{BaTiO}_3$
  - $\text{Bi}_2\text{O}_3/\text{SrTaO}_6/\text{SrTiO}_3$
  - $\text{Bi}_2\text{O}_3/\text{Bi}_2\text{Ti}_3\text{O}_9$
  - $(\text{Bi}_4\text{Ti}_3\text{O}_{12})$  : BIT

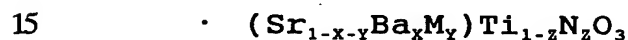
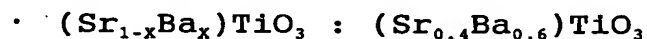
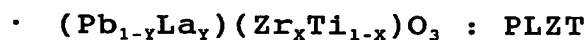
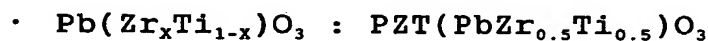
In the case of  $n = 4$  :

- 25
- $\text{Bi}_2\text{O}_3/\text{Sr}_3\text{Ti}_4\text{O}_{12}$

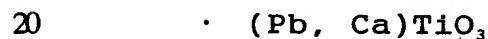
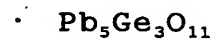
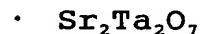
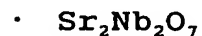


Although the bismuth based system layered structure  
 5 ferroelectrics in the above-mentioned item ① are preferably  
 used as a material for the ferroelectric films 13, 27 and 43,  
 ferroelectrics composed of each of the following materials  
 can be also used.

② Ferroelectrics (of an isotropic material system)  
 10 expressed by the following general formula:



M is La, Bi, Sb or Y, and N is Nb, V, Ta, Mo or W.



#### (8) Method of forming ferroelectric film

It is possible to use, as a method of forming the  
 ferroelectric films 13, 27 and 43, a molecular beam epitaxy  
 (MBE) method, a laser ablation method, a laser molecular beam  
 25 epitaxy method, a sputtering method (of an RF (Radio

Frequency) type, a DC (Direct Current) type, or an ion beam type), a reactive evaporation method, an MOCVD (Metal Organic Chemical Vapor Deposition) method, a mist deposition method, a sol-gel method, etc.

5       (9) Another modified example

A material for the gate electrode 3 and the connecting layer 10 is not limited to polysilicon or W. The other conductive material may be used.

Although in the above-mentioned embodiment, the FET is  
10 formed on the silicon substrates 1 and 21, the FET may be formed on the other semiconductor substrate or semiconductor layer.

Although in the above-mentioned embodiment,  
description was made of the ferroelectric memory having an  
15 n-type channel, a ferroelectric memory having a p-type channel is also realized by reversing the conductivity type of each layer.

The present invention is not limited to the ferroelectric memory in the above-mentioned embodiment. For  
20 example, it is applicable to various ferroelectric memories each having a ferroelectric capacitor.

Although in the above-mentioned embodiment,  
description was made of a case where the present invention  
is applied to the ferroelectric capacitor in the  
25 ferroelectric memory which operates as a nonvolatile memory,

the present invention is also applicable to a ferroelectric capacitor in a ferroelectric memory which performs nonvolatile operations.

Furthermore, the present invention is also applicable  
5 to the formation of a dielectric capacitor having a structure in which a dielectric film is interposed between conductive layers, or another dielectric device having a structure in which a dielectric film and a conductive layer are laminated.

Although the present invention has been described and  
10 illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.